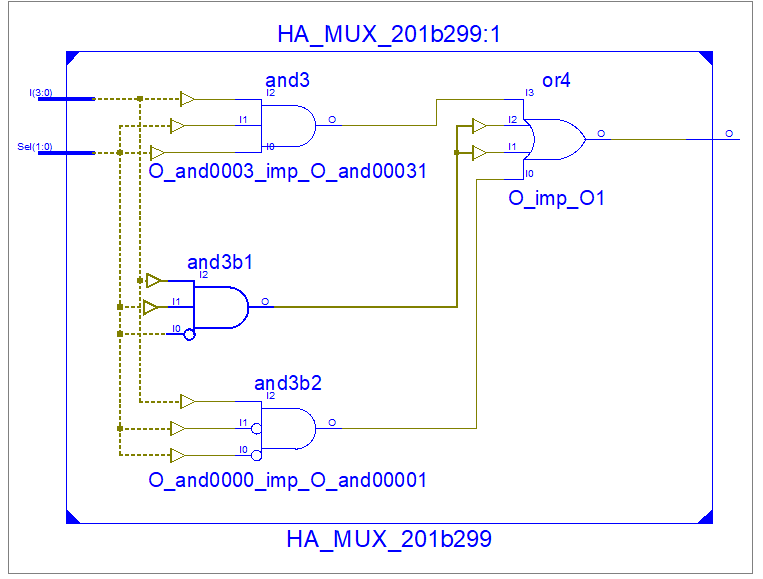
**EXPERIMENT 4**

**Exercise#1:** Design a half adder using two 4:1 multiplexers (shown in Fig.1) in structural style of architecture.

**Design Code (MUX):**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity HA\_MUX\_201b299 is

Port ( I : in STD\_LOGIC\_VECTOR (3 downto 0);

Sel : in STD\_LOGIC\_VECTOR (1 downto 0);

O : out STD\_LOGIC);

end HA\_MUX\_201b299;

architecture structural of HA\_MUX\_201b299 is

begin

O <= (not Sel(1) and (not Sel(0)) and I(0))

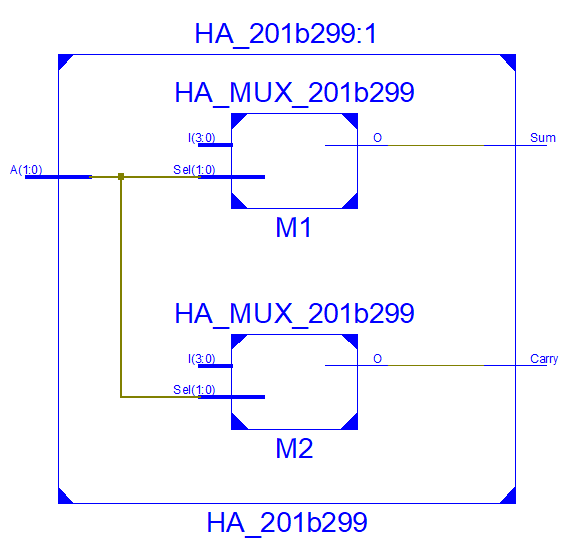
or (not Sel(1) and Sel(0) and I(1))

or (Sel(1) and (not Sel(0)) and I(2))

or (Sel(1) and Sel(0) and I(3));

end structural;

**Design Code (Half Adder):**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity HA\_201b299 is

Port ( A : in STD\_LOGIC\_VECTOR (1 downto 0);

Sum : out STD\_LOGIC;

Carry : out STD\_LOGIC);

end HA\_201b299;

architecture Structural of HA\_201b299 is

component HA\_MUX\_201b299

Port ( I : in STD\_LOGIC\_VECTOR (3 downto 0);

Sel : in STD\_LOGIC\_VECTOR (1 downto 0);

O : out STD\_LOGIC);

end component HA\_MUX\_201b299;

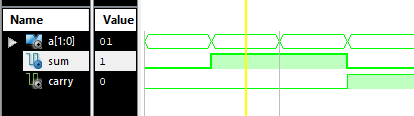
begin

-- porting

M1: HA\_MUX\_201b299 port map ("0110", A, Sum );

M2 : HA\_MUX\_201b299 port map("0001", A, Carry);

end Structural;

**Test Bench Code:**

A <= "00";

wait for 100 ns;

A <= "01";

wait for 100 ns;

A <= "10";

wait for 100 ns;

A <= "11";

wait for 100 ns;

**Exercise#2:** Design 8:1 multiplexer using two 4:1 and one 2:1 multiplexers (shown in Fig.2) in structural style of architecture. Use inputs and selection lines in the form of bus.

**Design code (2x1 MUX):**

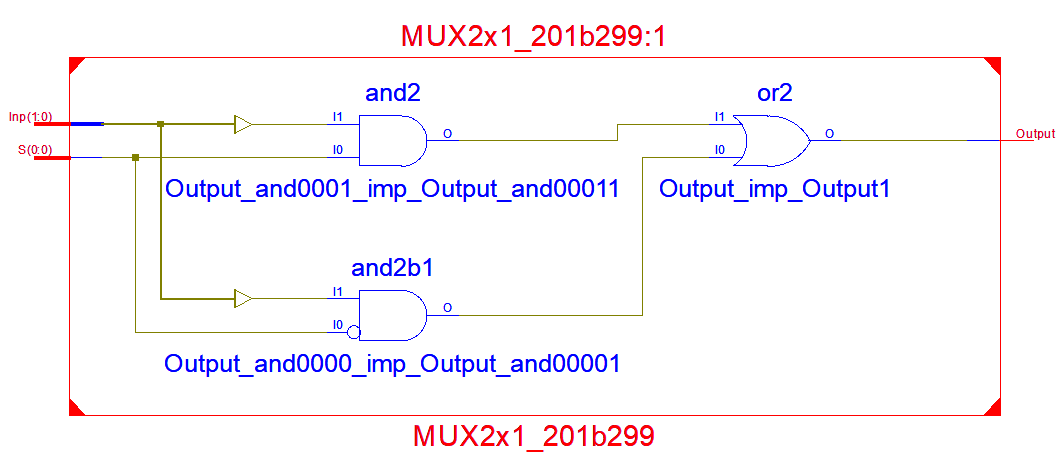
library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity MUX2x1\_201b299 is

Port ( Inp : in STD\_LOGIC\_VECTOR (1 downto 0);

S : in STD\_LOGIC\_VECTOR (0 downto 0);

 Output : out STD\_LOGIC);

end MUX2x1\_201b299;

architecture Behavioral of MUX2x1\_201b299 is

begin

Output <= (not S(0) and Inp(0))

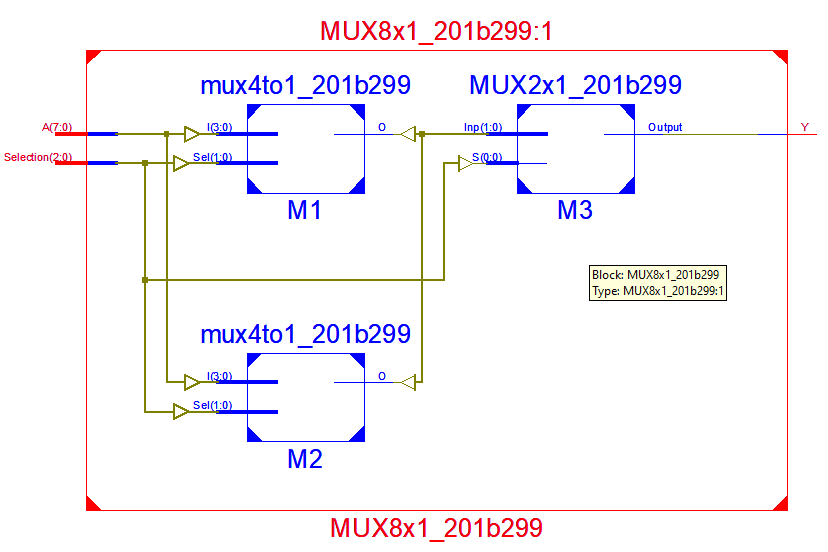
or (S(0) and Inp(1));

end Behavioral;

**Design code (8x1 MUX):**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;



entity MUX8x1\_201b299 is

Port ( A : in STD\_LOGIC\_VECTOR (7 downto 0);

Selection : in STD\_LOGIC\_VECTOR (2 downto 0);

Y : out STD\_LOGIC);

end MUX8x1\_201b299;

architecture Structural of MUX8x1\_201b299 is

component mux4to1\_201b299

Port ( I : in STD\_LOGIC\_VECTOR (3 downto 0);

Sel : in STD\_LOGIC\_VECTOR (1 downto 0);

O : out STD\_LOGIC);

end component mux4to1\_201b299;

component MUX2x1\_201b299

Port ( Inp : in STD\_LOGIC\_VECTOR (1 downto 0);

S : in STD\_LOGIC\_VECTOR (0 downto 0);

Output : out STD\_LOGIC);

end component MUX2x1\_201b299;

signal Sig: STD\_LOGIC\_VECTOR (1 downto 0);

begin

-- porting

M1 : mux4to1\_201b299 port map(A(3 downto 0), Selection(1 downto 0), Sig(0));

M2 : mux4to1\_201b299 port map(A(7 downto 4), Selection(1 downto 0), Sig(1));

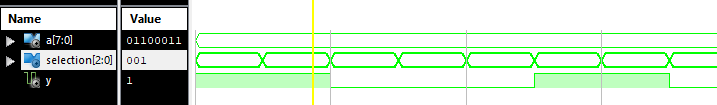
M3 : MUX2x1\_201b299 port map(Sig(1 downto 0), Selection(2 downto 2), Y);

end Structural;

**Test Bench Code:**

A <= "01100011";

Selection <= "000";

wait for 100 ns;

Selection <= "001";

wait for 100 ns;

Selection <= "010";

wait for 100 ns;

Selection <= "011";

wait for 100 ns;

Selection <= "100";

wait for 100 ns;

Selection <= "101";

wait for 100 ns;

Selection <= "110";

wait for 100 ns;

Selection <= "111";

wait for 100 ns**;**